## REMARKS

The above Amendments and these Remarks are in reply to the Office Action mailed August 4, 2006.

Currently, claims 1-36 are pending. Applicants respectfully request reconsideration of claims 1-36.

### I. Summary of the Examiner's Objections

Claims 1-15 were rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement.

Claims 1-3, 5-17, 19, 20, and 25-36 were rejected under 35 U.S.C. § 102(e) as being anticipated by *Lee* (USP 6,795,366).

Claims 4 and 18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Lee* (USP 6,795,366) in view of *Hellums* (5,362,988).

Claims 21-24 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Lee* (USP 6,795,366).

### II. Summary of the Amendments

Applicant has amended claims 1, 2, 16, 25, 32, 33, and 34 herein.

### III. Remarks

#### A. Summary of Examiner Teleconference

The Examiner is thanked for the opportunity to discuss this application with the undersigned Attorney on November 2, 2006. Clarification of the Examiner's Response to Arguments set forth at pages 7 and 8 of the outstanding Office Action was discussed.

It was noted by Applicant's Attorney that a difference between the *Lee* (USP 6,795,366) and the subject matter of the instant application is that in *Lee*, a bypass is turned on during power up and turned off when the external voltage supply reaches an operating level voltage. In contrast, in the

present subject matter, the bypass is turned off during power up and subsequently turned on once the host has completed ramping its supply voltage to the memory device.

The Examiner suggested clarification of the "power up complete signal" limitation.

No agreement on allowability of the claims was reached.

**B. Rejections Under 35 U.S.C. § 112**

It is respectfully submitted that the limitations calling for "a bypass enable signal outputted by the controller subsequent to the power up complete signal being generated by the host device indicating that power of the host is complete" is supported by the specification. As understood, this rejection relates to the host generating "a power up complete signal" portion of the limitation.

This limitation is supported by at least paragraphs 39, 41 and 42. A control signal is provided by the host device to indicate power of completion:

> "A control signal from the host is then utilized to indicate power-up completion, and the output of the sampling logic then used to determine whether to implement the BYPASS signal. (Paragraph 39).
>
> . . . at step 720, with the bypass set to off, the controller waits for a indicator signal from the host device that power up has been completed. (Paragraph 41).
>
> . . . at Step 730, upon receipt of the power up signal from the host device, the sampling logic 520 will test the output of the low voltage comparator 510." (Paragraph 42).

Hence, it is respectfully submitted that the rejection under 35 U.S.C. § 112 should be withdrawn.

**C. Rejections Under 35 U.S.C. §102**

As indicated during the telephonic interview, at least one fundamental difference exists between the claimed invention and *Lee*: *Lee* enables the bypass during power-up or ramping of an external voltage supplied to the memory device. In contrast, the claimed invention enables a bypass only "... subsequent to the power of complete signal being generated by the host device indicating that the host voltage has reached the level..." suitable for operation of the memory system. In other words, in the present invention, the bypass is enabled when the host has completed its power-up

cycle while *Lee*'s is disabled after power-up.

During our teleconference, the Examiner indicated that the term "power up complete signal" might be better defined. Accordingly, the independent claims have been amended to define that the "power of complete signal" indicates "that the host voltage has reached . . . a level suitable for operation of the memory system" (claim 1); or that "the power-up completion signal indicating that the host voltage is at a level suitable for operation of the memory system" (claim 16). Similar limitations are present in independent claims 25, 32 and 34:

> a bypass control signal output from the controller coupled to the bypass element and ***responsive to a host system power up completed signal indicating that the host voltage is at a level suitable for operation of the memory system*** and which enables the bypass element when the host voltage is below a threshold level subsequent to host power-up completion (Claim 25). (Emphasis Supplied)
>
> --or--
>
> ***responsive to a command signal from the host device indicating that the host voltage is at a level suitable for operation of the memory system***, determining the power supplied by the host; and
> if the power is below a threshold operating voltage ***subsequent to the command signal***, enabling the bypass using the controller (Claim 32). (Emphasis Supplied)
>
> --or--
>
> a voltage regulator having a shorting element between a host voltage input and an output, the shorting element being ***responsive to a bypass control signal, the bypass control signal provided by the controller responsive to a host system power up complete signal indicating that the host voltage is at a level suitable for operation of the memory system*** which enables the shorting element when the host supply voltage provided by the host is below a threshold level subsequent to power-up completion. (Claim 34). (Emphasis Supplied)

It is respectfully submitted that no such power-up complete signal exists in the *Lee* reference. The Examiner as asserted that a signal at element N1 prior to time T1 in Figure 17 causes the output of inverter INV2 to cause a vertical ramping of the internal voltage, and therefore may comprise a power-up completion signal. *Lee* clearly teaches that this signal occurs at a time prior to completion of the ramping of the external voltage (Vext) to its maximum (subsequent to time T1). (Figure 17)

If Vext is equivalent to the "host voltage" in the independent claims, this signal occurs prior to Vext reaching is level suitable for device operation as indicated by the generation of signal (PDT) which occurs when the external voltage reaches a level sufficient to cause PDT to go to a logic level low. (See *Lee* discussion at Figures 7 and 8.)

Hence, this signal at node N1 which the Examiner relies on as comprising a power of complete signal, cannot comprise a "power up complete signal" which indicates that the host voltage has reached a level suitable for operating a memory system as defined in the present claims. Any such signal at N1 only occurs when Vext reaches a level sufficient to operate the device and PDT goes to a logic level low as indicated in the discussion of Figure 7 and 8 and in columns 3, line 39 through column 3, line 64 of *Lee*.

It is therefore respectfully submitted each and every limitation of the claimed invention as defined in claims 1, 16, 25, 32, and the claims dependent therefrom, is not disclosed in the *Lee* reference. Hence, it is respectfully submitted that the claims are not anticipated by *Lee*.

**D. Rejections Under 35 U.S.C. §103**

It is respectfully submitted that claims 4 and 18 are not obvious under 35 U.S.C. § 103(a) over *Lee* in view of *Hellums* (U.S. Patent No 5,362,988). It is further respectfully submitted that claims 21 – 24 are not obvious under 35 U.S.C. § 103(a) over *Lee*.

*Hellums* is cited by the Examiner as teaching that a transistor can be comprised of a plurality of transistors. However, *Hellums* adds nothing to dissuade one of average skill from the direct teaching of *Lee* that one enables the bypass to achieve the advantage of providing "a quickly ramped-up internal supply voltage… within the system required time". In contrast, the advantage of the present invention is that over-voltage protection is achieved by not enabling the bypass until a power up complete signal is received and the supply voltage is below a threshold.

Hence, neither *Lee* nor *Hellums* alone or in combination would teach one of average skill in the art to make the claimed invention including a "power up complete" signal as presently claimed.

Still further, Claims 21 – 24 are not obvious in view of *Lee* alone. As noted above, *Lee* maintains the bypass as enabled when the threshold voltage is below a particular level. When a

power up completed signal is received, *Lee* disables the bypass. Hence, *Lee* acts in direct contradiction to the claimed invention.

Hence, it is respectfully submitted claims 4, 18, and 21 – 24 are not obvious in view of *Lee*.

**E. Request For Entry And Consideration Of Amendment**

Entry of the foregoing amendments is respectfully requested and it is submitted that such amendments are in compliance with 37 C.F.R. § 1.116. The amendment presents the claims in a better form for consideration on appeal. In addition, the amendment is necessary and was not earlier presented because the examiner's lack of clarity with respect to the term "power-up complete signal", was not set forth in the Office Action.

The Examiner's prompt attention to this matter is greatly appreciated. Should further questions remain, the Examiner is invited to contact the undersigned attorney by telephone.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 501826 for any matter in connection with this response, including any fee for extension of time, which may be required.

Respectfully submitted,

Date: November 6, 2006

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